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(21)Application number : 06-174972	(71)Applicant : NEC CORP
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(54) SWITCHING POWER-SUPPLY CIRCUIT

(57)Abstract:

PURPOSE: To obtain a switching power-supply circuit in which a loss caused by the operating delay of a MOS5ET for synchronous rectification with reference to the operation of a main switch is reduced to a minimum under various input conditions and various load conditions in a switching power supply which uses the MOSFET for a rectifying operation.

CONSTITUTION: Control-signal levels V0 to V2 which correspond to an output voltage generated by a control circuit 26 and triangular waves V3 are level- compared by respective comparators 19 to 22, and respective switching elements 3 to 5 are ON-OFF-controlled by using respective comparison output pulses P0 to P2.At this time, the control-signal level V1 is level-shifted sequentially by constant values (VCE,1, VCE2) by means of transistors 12, 13 in a saturated state, and the control-signal levels V0, V2 are generated. Since the control-signal levels V0, V2 are level-shifted by the constant values with reference to the control-signal level 1, the dead time in an ON-OFF-operation of the switching elements 3, 4, 5 can be maintained constant irrespective of an input/output condition.
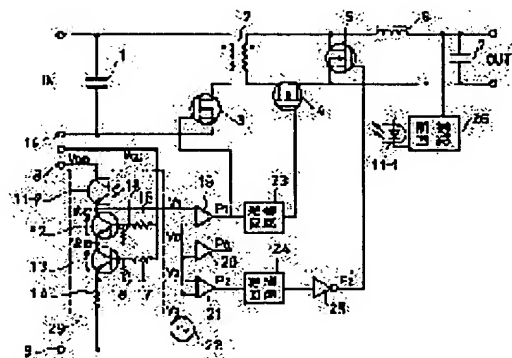
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(54)【発明の名称】　スイッテング電源回路

(57)【要約】

【目的】　ＭＯＳＦＥＴを整流用として用いたスイッチング電源において、種々の入力条件．負荷条件の下で主スイッチの動作に対する同期整流用ＭＯＳＦＥＴの動作遅れに起因する損失を最小とする。

【構成】　制御回路26により発生される出力電圧に応じた制御信号レベル$V_0 \sim V_2$と三角波V_3とを各比較器19～22によりレベル比較して．各比較出力パルス$P_0 \sim P_2$を用いて各スイッチ素子3～5をオンオフ制御する。このとき、飽和状態のトランジスタ12，13により、制御信号レベルV_1を順次一定値（V_{CE1}，V_{CE2}）づつレベルシフトしてV_0，V_2を生成する。

【効果】　V_1に対してV_0，V_2が一定値づつレベルシフトしたものであるので．入出力条件にかかわらず、スイッチ素子3と4，5のオンオフ時のデッドタイムは一定に維持される。
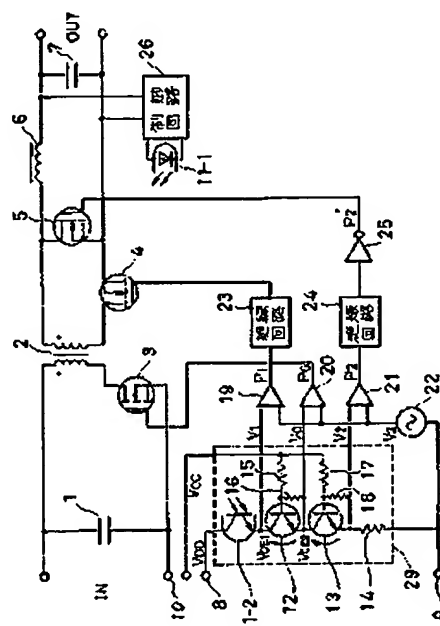
【特許請求の範囲】

【請求項1】　トランスと、このトランスの一次側供給電力をスイッチングする主スイッチ素子と、前記トランスの二次側出力電力を整流平滑する整流平滑手段と、この整流平滑手段に設けられ前記主スイッチ素子のオンオフ動作と略同期してオンオフ制御される同期整流用スイッチ素子とを含むスイッチング電源回路であって、

三角波発を発生する手段と、

前記整流平滑手段の出力レベルに応じた直流制御信号のレベルを一定レベルだけレベルシフトしてレベルシフト電圧を生成するレベルシフト手段と、

前記直流制御信号と前記三角波とのレベル比較を行ってこの比較パルスを前記同期整流用スイッチ素子のスイッチングパルスとする手段と、

前記レベルシフト電圧と前記三角波とのレベル比較を行ってこの比較パルスを前記主スイッチ素子のスイッチングパルスとする手段と、

を含むことを特徴とするスイッチング電源回路。

【請求項2】　トランスと、このトランスの一次側供給電力をスイッチングする主スイッチ素子と、前記トランスの二次側出力電力を整流平滑する整流平滑手段と、この整流平滑手段内において前記トランスの二次巻線に夫々直列及び並列接続されて前記主スイッチ素子のオンオフ動作と略同期してオンオフ制御される第1及び第2の同期整流用スイッチ素子とを含むスイッチング電源回路であって、

三角波発を発生する手段と、

前記整流平滑手段の出力レベルに応じた直流制御信号のレベルを順次一定レベルずつレベルシフトして第1及び第2のレベルシフト電圧を生成するレベルシフト手段と、

前記直流制御信号と前記三角波とのレベル比較を行ってこの比較パルスを前記第1の同期整流用スイッチ素子のスイッチングパルスとする手段と、

前記第1のレベルシフト電圧と前記三角波とのレベル比較を行ってこの比較パルスを前記主スイッチ素子のスイッチングパルスとする手段と、

前記第2のレベルシフト電圧と前記三角波とのレベル比較を行ってこの比較パルスを前記第2の同期整流用スイッチ素子のスイッチングパルスとする手段と、

を含むことを特徴とするスイッチング電源回路。

【請求項3】　前記レベルシフト手段は互いに直列接続された第1及び第2のトランジスタと、これ等各トランジスタを飽和動作状態に夫々バイアスするバイアス手段とを含むことを特徴とする請求項1または2記載のスイッチング電源回路。

【請求項4】　前記レベルシフト手段は、前記整流平滑手段の出力レベルに応じてインピーダンスが変化自在な可変インピーダンス素子と前記第1及び第2のトランジスタとがこの順に電源間に直列接続された構成であること

とを特徴とする請求項3記載のスイッチング電源回路。

【請求項5】　前記可変インピーダンス素子と前記第1のトランジスタの直列接続点の電圧レベルが前記直流制御信号レベルであることを特徴とする請求項4記載のスイッチング電源回路。

【請求項6】　前記整流平滑手段の出力レベルに応じて光信号を生成する手段と、この光信号を受光してこの光信号に応じたインピーダンスを呈する受光素子とを含み、この受光素子が前記可変インピーダンス素子であることを特徴とする請求項4または5記載のスイッチング電源回路。

【請求項7】　前記スイッチングパルスの各々を対応スイッチ素子のゲートへ供給するフォトカプラを含むことを特徴とする請求項6記載のスイッチング電源回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明はスイッチング電源回路に関し、特に整流部にMOSFET同期整流回路を用いたスイッチング電源回路に関するものである。

【0002】

【従来の技術】スイッチング電源回路の整流部における損失を低減することを目的として、MOSFETによる同期整流方式が採用されている。図7はこの同期整流方式を用いたスイッチング電源回路の一例を示すものである。

【0003】図において、トランス2の一次側には入力電力が、主スイッチ素子であるMOSFET3を介してオンオフ制御されることにより印加される。このトランス2の二次側に誘起される交流電力は整流用のMOSFET4、5により整流され、チョークコイル6及びコンデンサ7により平滑化されて直流出力電圧に変換される。尚、1は入力コンデンサである。

【0004】整流回路部には、トランス2の二次巻線に直列の整流用MOSFET4と二次巻線に並列の転流用（フライホイール用）のMOSFET5とが設けられており、これ等MOSFET4、5は基本的には主スイッチ素子3のオンオフと同期してオンオフする様に制御されるものである。

【0005】更に詳述すれば、主スイッチ素子3がオンのとき整流用MOSFET4はオンとなり、転流用MOSFET5はオフとなる。また、主スイッチ素子3がオフのとき、整流用MOSFET4はオフとなり、転流用MOSFET5はオンとなる。

【0006】すなわち、主スイッチ素子3がオンのとき、MOSFET4がオンとなり、MOSFET5がオフとなるから、電源の入力INから出力OUTへエネルギの供給が行われる。また、主スイッチ素子3がオフのとき、MOSFET4はオフとなり、MOSFET5はオンとなって、チョークコイル6の蓄積エネルギにより電源の出力OUTへエネルギが供給されることになる。

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【0007】これ等スイッチ素子3〜5のオンオフ制御パルスを生成する駆動回路について説明する。整流平滑電圧が制御回路26へ入力され、この電圧レベルに応じた電気信号がフォトカプラの発光素子11−1により光信号に変換されて受光素子11−2へ印加される。

【0008】この受光素子11−2はこの光の強弱に従ってそのインピーダンスが変化する可変インピーダンス素子である。この可変インピーダンス素子11−2と、抵抗27、28、14とがこの順に電源8、9に直列に接続され、制御信号出力回路29を構成している。

【0009】これ等各直列接続点からの出力電圧V0〜V2が制御信号となって導出されており、これ等各制御信号レベルV0〜V2と三角波発生器22による三角波レベルV3とが比較器19〜21にて夫々比較される。

【0010】可変インピーダンス素子11−2と抵抗27との直列接続点の制御信号レベルV1は比較器19にて三角波レベルV3と比較され、この比較出力パルスP1が絶縁回路23を介してMOSFET4のゲート制御パルスとなっている。

【0011】抵抗27と28との直列接続点の制御信号レベルV0は比較器20にて三角波レベルV3と比較され、この比較出力パルスP0が主スイッチ素子3のゲート制御パルスとなっている。

【0012】また、抵抗28と14との直列接続点の制御信号レベルV2は比較器21にて三角波レベルV3と比較され、この比較出力パルスP2が絶縁回路24及びインバータ25を介してMOSFET5の制御パルスP2′となっている。

【0013】尚、絶縁回路23、24はフォトカプラが用いられており、制御回路26の出力信号を制御信号出力回路29へ伝達するフォトカプラ（11−1、11−2）と共に、トランス2の一／二次間の絶縁を行っている。

【0014】次に、動作について説明する。図8は図7の回路の各部動作波形図である。制御回路26の出力信号をフォトカプラ発光側11−1によりフォトカプラ受光側11−2へ伝達し、フォトカプラ受光側11−2のインピーダンスを変化させ、フォトカプラ受光側11−2と抵抗27の接続点の電圧V1、抵27と抵抗28の接続点の電圧V0、抵抗28と抵抗14の接続点の電圧V2を変化させ、これ等の電圧V1、V0、V2を三角波V3と比較することにより、比較器19、20、21の出力パルスP1、P0、P2のパルス幅を制御している。

【0015】このとき、V1＞V0＞V2の関係は常に保たれるので、パルスP1、P0、P2のオン時間をTON1、TON0、TON2とすると、TON1＜TON0＜TON2の関係は常に保たれる。

【0016】パルスP1によりFET4のゲートを駆動し、パルスP0により主スイッチ素子3のゲートを駆動

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し、パルスP2を反転器25で反転させたパルスP2′によりFET5のゲートを駆動する。

【0017】ここで、パルスP0がオンする時刻をt0、パルスP1がオンする時刻をt1、パルスP1がオフする時刻をt2、パルスP0がオフする時刻をt3、パルスP2′がオンする時刻をt4、パルスP2′がオフする時刻をt5とし、t1−t0＝t3−t2＝TD1（パルスP0、P1間デッドタイム）、t4−t3＝t0−t5＝TD2（パルスP0、P2′間デッドタイム）とする。

【0018】時刻t0〜t1間及びt2〜t3間は、主スイッチ3がオン、FET4、5がオフであり、トランス2の二次巻線→コイル6→負荷→FET4の内部ダイオード→トランス2の二次巻線のルートで負荷電流が流れる。

【0019】時刻t1〜t2間は、主スイッチ3、FET4がオン、FET5がオフであり、トランス2の二次巻線→コイル6→負荷→FET4→トランス2の二次巻線のルートで負荷電流が流れる。

【0020】時刻t3〜t4間及びt5〜t0間は主スイッチ3、FET4、5がオフであり、コイル6→負荷→FET5の内部ダイオード→コイル6のルートで負荷電流が流れる。時刻t4〜t5間は、主スイッチ3、FET4がオフ、FET5がオンであり、コイル6→負荷→FET5→コイル6のルートで負荷電流が流れる。

【0021】主スイッチ3の動作に対するFET4、5のオンの遅れは、FET4、5の内部ダイオードに負荷電流が流れることによりFET4、5の導通損失及びリカバリィ電流による損失を引き起こし、主スイッチ3の動作に対するFET4、5のオフの遅れは、トランス2の二次巻線短絡により主スイッチ3、FET4、5の短絡損失を引き起こす。

【0022】そこで、本例では、パルスP0がオフする直前にパルスP1をオフし、パルスP0がオンする直前にパルスP2′をオフすることにより、主スイッチ3の動作に対するFET4、5のオフの遅れに起因する損失を低減できるようにしている。パルスP0、P1、P2間に最適なデッドタイムTD1、TD2を設けることにより、電源の効率を最大にできることになる。

【0023】
【発明が解決しようとする課題】この従来のMOSFET同期整流用駆動回路を用いたスイッチング電源回路では、主スイッチの動作に対する同期整流用MOSFET4、5の動作の遅れ時間から最適なデッドタイムTD1、TD2が存在するが、電源の入力条件、負荷条件が変化した場合、この最適なデッドタイムTD1、TD2を維持することができなくなり、電源の効率が低下するという問題があった。

【0024】定格入力電圧・出力電流にて電源の効率が最大得られるようにデッドタイムTD1、TD2を設定し

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（図8（a））．例えば電源の入力電圧が上昇した場合
（図8（b））．主スイッチのパルス幅を絞るため主ス
イッチのパルス幅を制御する直流電圧Ｖｇが上昇する。
このときフォトカプラ受光側11－2のインピーダンス
が小さくなり．抵抗27，28を流れる電流が増加する
ため．直流電圧ＶｇとＦＥＴ4，5のパルス幅を制御す
る直流電圧Ｖ1，Ｖ2との電圧差が増加し、デッドタイ
ムＴＤ1．ＴＤ2がＴＤ1′，ＴＤ2′に増加し、最適なデッド
タイムを維持することができなくなる。よって．ＦＥＴ
4，5の内部ダイオードの導通時間が増加し、ＦＥＴ
4，5の導通損失およびリカバリィ電流による損失が増
加し．電源の効率が低下することになる。

【0025】本発明の目的は、入出力条件の変化にかか
わらず最適なデッドタイムを常時維持可能として電源効
率を良好とし得るスイッチング電源回路を提供すること
である。

【0026】
【課題を解決するための手段】本発明によれば．トラン
スと．このトランスの一次側供給電力をスイッチングす
る主スイッチ素子と、前記トランスの二次側出力電力を
整流平滑する整流平滑手段と、この整流平滑手段に設け
られ前記主スイッチ素子のオンオフ動作と略同期してオ
ンオフ制御される同期整流用スイッチ素子とを含むスイ
ッチング電源回路であって．三角波を発生する手段
と．前記整流平滑手段の出力レベルに応じた直流制御信
号のレベルを一定レベルだけレベルシフトしてレベルシ
フト電圧を生成するレベルシフト手段と、前記直流制御
信号と前記三角波とのレベル比較を行ってこの比較パル
スを前記同期整流用スイッチ素子のスイッチングパルス
とする手段と、前記レベルシフト電圧と前記三角波との
レベル比較を行ってこの比較パルスを前記主スイッチ素
子のスイッチングパルスとする手段と、を含むことを特
徴とするスイッチング電源回路が得られる。

【0027】更に本発明によれば、トランスと．このト
ランスの一次側供給電力をスイッチングする主スイッチ
素子と、前記トランスの二次側出力電力を整流平滑する
整流平滑手段と．この整流平滑手段内において前記トラ
ンスの二次巻線に夫々直列及び並列接続されて前記主ス
イッチ素子のオンオフ動作と略同期してオンオフ制御さ
れる第1及び第2の同期整流用スイッチ素子とを含むス
イッチング電源回路であって、三角波を発生する手段
と．前記整流平滑手段の出力レベルに応じた直流制御信
号のレベルを順次一定レベルずつレベルシフトして第1
及び第2のレベルシフト電圧を生成するレベルシフト手
段と、前記直流制御信号と前記三角波とのレベル比較を
行ってこの比較パルスを前記第1の同期整流用スイッチ
素子のスイッチングパルスとする手段と、前記第1のレ
ベルシフト電圧と前記三角波とのレベル比較を行ってこ
の比較パルスを前記主スイッチ素子のスイッチングパル
スとする手段と．前記第2のレベルシフト電圧と前記三

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角波とのレベル比較を行ってこの比較パルスを前記第2
の同期整流用スイッチ素子のスイッチングパルスとする
手段と、を含むことを特徴とするスイッチング電源回路
が得られる。

【0028】
【作用】スイッチング電源出力である整流平滑電圧レベ
ルに応じた直流制御信号レベルを一定レベルだけレベル
シフトしてレベルシフト電圧を生成し、このレベルシフ
ト電圧と直流制御信号との各レベルを三角波レベルと夫
々比較して比較出力パルスを得る。これ等比較出力パル
スを主スイッチ素子や整流用スイッチ素子のオンオフパ
ルスとする。

【0029】
【実施例】以下．図面を用いて本発明の実施例について
説明する。

【0030】図1は本発明の一実施例の回路図であり、
図7と同等部分は同一符号により示している。図7と異
なる部分についてのみ説明し、その他の構成については
省略する。

【0031】制御信号出力回路29において、電源8－
9間に可変インピーダンス素子としての受光素子11－
2と．ＮＰＮトランジスタ12，13と、抵抗14とが
この順に直列接続して設けられている。これ等トランジ
スタ12，13のベースエミッタ間には、電源Ｖｃｃから
抵抗15，16および17，18によりバイアスが付与
されており、これ等電源Ｖｃｃ，Ｖｍ（電源8への印加電
源電圧）及び抵抗15～18の選定により、各トランジ
スタ12，13は飽和領域で動作するようになってお
り．よってトランジスタ12，13による電圧ドロップ
である電圧シフトレベルはＶＣＥ1，ＶＣＥ2（コレクタ・
エミッタ間飽和電圧）となり一定に維持されている。

【0032】そして、可変インピーダンス素子11－2
とトランジスタ12との直列点の電圧Ｖ1が三角波Ｖ3
と比較器19でレベル比較される。また、トランジスタ
12によりＶ1をＶＣＥ1だけレベルシフトした電圧Ｖｇ
が三角波Ｖ3と比較器20でレベル比較される。更に、
トランジスタ13によりＶｇをＶＣＥ2だけレベルシフト
した電圧Ｖ2が三角波Ｖ3と比較器21でレベル比較さ
れる。

【0033】次に動作について説明する。図2は図1の
回路の動作波形を示している。トランジスタ1，13は
トランジスタ駆動用電源10により駆動され、飽和状態
にて動作するが．ここでトランジスタ12，13のコレ
クタ・エミッタ間飽和電圧を夫々ＶＣＥ1，ＶＣＥ2とす
る。

【0034】出力電圧制御回路26の出力信号をフォト
カプラ発光側11－1によりフォトカプラ受光側11－
2へ伝達し、フォトカプラ受光側11－2のインピーダ
ンスを変化させ．フォトカプラ受光側11－2とトラン
ジスタ12のコレクタの接続点の電圧Ｖ1、トランジス

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タ12のエミッタとトランジスタ13のコレクタの接続点の電圧V0、トランジスタ13のエミッタと抵抗14の接続点の電圧V2を夫々変化させ、これ等の電圧V1、V0、V2を三角波V3と比較する。これにより、比較器19、20、21の出力パルスP1、P0、P2のパルス幅が制御される。

【0035】フォトカプラ受光側11−2のインピーダンスが変化し、トランジスタ12、13を流れる電流が変化しても、VCE1、VCE2は一定であり、

$V1 = V0 + VCE1 > V0 > V2 = V0 - VCE2$

の関係は常に保たれ、パルスP1、P0、P2のオン時間をTON1、TON0、TON2とすると、

$TON1 = TON0 - 2TD1 < TON0 < TON2 = TON0 + 2TD2$

の関係は常に保たれる（TD1；パルスP0、P1間デッドタイム、TD2；パルスP0、P2間デッドタイム）。

【0036】パルスP1によりFET4のゲートを駆動し、パルスP0により主スイッチ3のゲートを駆動し、パルスP2を反転器25で反転させたパルスP2´によりFET5のゲートを駆動する。

【0037】各時間における負荷電流の整流方法は従来回路図7と同様であり、説明は省略する。

【0038】本実施例では、パルスP0がオフする時刻より時間TD1だけ前の時刻にパルスP1をオフし、パルスP0がオンする時刻より時間TD2だけ前の時刻にパルスP2´をオフするが、主スイッチ3の動作に対するFET4、5の動作の遅れ時間をTDLYとすると、TD1、TD2≧TDLYとなるように電圧VCE1、VCE2を設定すると、主スイッチ3の動作に対するFET4、5のオフの遅れに起因する損失を零にすることができる。主スイッチ3の動作に対するFET4、5のオンの遅れに起因する損失を最小にすることができる。

【0039】TD1、TD2＝TDLYとなるようにトランジスタ12、13のコレクタ・エミッタ間飽和電圧VCE1、VCE2を抵抗15または16、抵抗17または18により設定する。

【0040】ここで定格入力電圧・出力電流にて電源の効率が最大得られるようにデッドタイムTD1、TD2を設定し（図2（a））、例えば電源の入力電圧が上昇した場合（図2（b））、主スイッチ3のパルス幅を絞るため主スイッチ3のパルス幅を制御する直流電圧V0が上昇するが、このとき直流電圧V0とFET4、5のパルス幅を制御する直流電圧V1、V2との差分は夫々VCE1、VCE2で一定であるため、デッドタイムTD1、TD2は一定であり、最適なデッドタイムを維持することができる。従って、電源の入力条件、負荷条件が変化しても、常に最適なデッドタイムを維持することができ、電源の効率を最大に維持できる。

【0041】図3は本発明の図1の実施例と従来の図7の例との各々において、同一条件で制御信号レベルV1

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とデッドタイムTD1、TD2との関係を示したものである。

【0042】入力電圧48V（IN）、出力電圧3.3V（OUT）、出力電流3.6A、スイッチング周波数300KHzのフォードコンバータとし、FET4、5には入力容量1200pF、オン抵抗4.5mΩのMOSFETを用いており、従来例ではデッドタイムが特性31の如く、制御信号レベルV1に比例して変化するが、本例では、特性30の如く常時一定のデッドタイムが得られることが判る。

【0043】尚、レベルシフト用としてトランジスタ12、13の飽和電圧を用いているが、ツェナーダイオードを用いて一定のレベルシフト電圧を得ても良いことは明らかである。

【0044】図4は本発明の他の実施例の回路図であり、トランジスタ12、13の駆動用バイアス電源として制御信号出力回路29の電源8（VDD）を用いて共用化したものである。

【0045】図5は本発明の更に他の実施例の回路図であり、PNPトランジスタ12、13を用いたもので、図6はこれ等PNPトランジスタ12、13の駆動用バイアス電源を制御信号出力回路29の電源と共用化したものである。

【0046】

【発明の効果】以上述べた如く、本発明によれば、スイッチ素子のオンオフパルスを得るための制御信号レベルを一定レベルシフトした電圧により得ているので、電源の入力条件や出力条件に依存しない一定のデッドタイムを、主スイッチ素子と同期整流用スイッチ素子とのオンオフ周期内に設けることができ、よって主スイッチ素子の動作に対して同期整流用MOSFETの動作遅れに起因する損失を常に最小にすることが可能となって電源効率が最大になるという効果がある。

【図面の簡単な説明】

【図1】本発明の一実施例の回路図である。

【図2】図1の回路の動作を示す波形図であり、（a）は電源の入出力条件が定格の場合、（b）は電源の入力電圧が高くなった場合の各波形図である。

【図3】制御信号レベルとデッドタイムとの関係を本発明と従来例とで比較して示した図である。

【図4】本発明の他の実施例の回路図である。

【図5】本発明の別の実施例の回路図である。

【図6】本発明の更に別の実施例の回路図である。

【図7】従来のスイッチング電源回路を示す図である。

【図8】図7の回路の動作を示す波形図であり、（a）は電源の入出力条件が定格の場合、（b）は電源の入力電圧が高くなった場合の各波形図である。

【符号の説明】

1　　入力コンデンサ

2　　トランス

(5)　　　　　　　　　　　　　　　　　特開平8－37777

3	主スイッチ素子	＊14	抵抗
4，5	同期整流用スイッチ素子	15～18	バイアス抵抗
6	チョークコイル	19～21	比較器
7	出力コンデンサ	22	三角波
11－1	発光素子	23，24	絶縁回路
11－2	受光素子	25	インバータ
12，13	トランジスタ	＊	

【図1】

【図2】

(a)　　　　　　　(b)
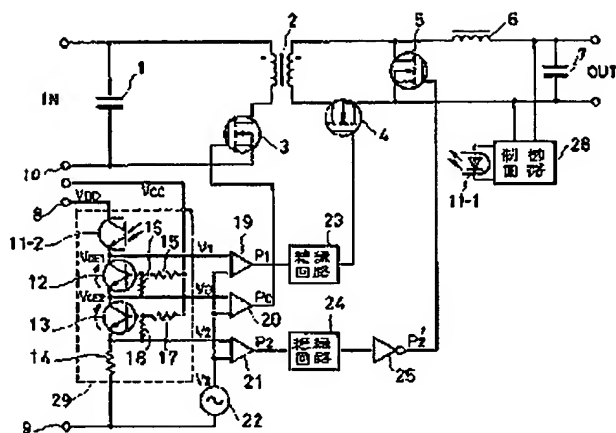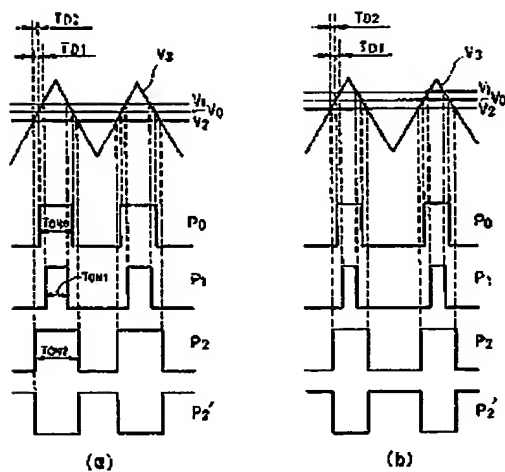
【図3】
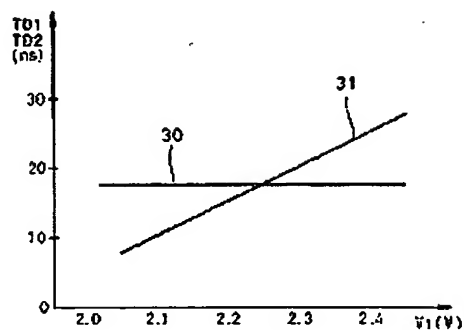
(7)　　　　　　　　　特開平8−37777

【図4】

【図5】

(8)   特開平8-37777

【図6】

【図7】

(9)

特開平8－37777

【図8】

(a)

(b)

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
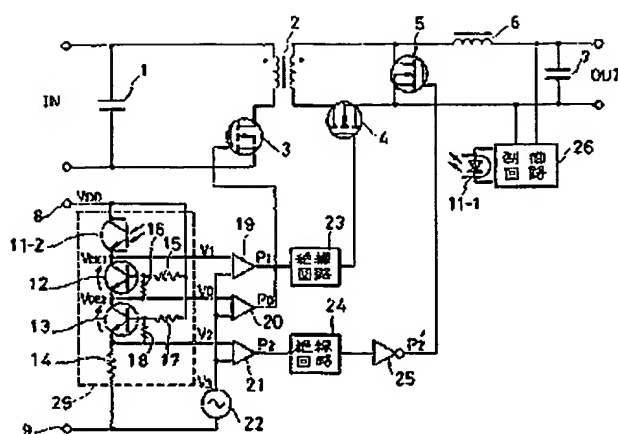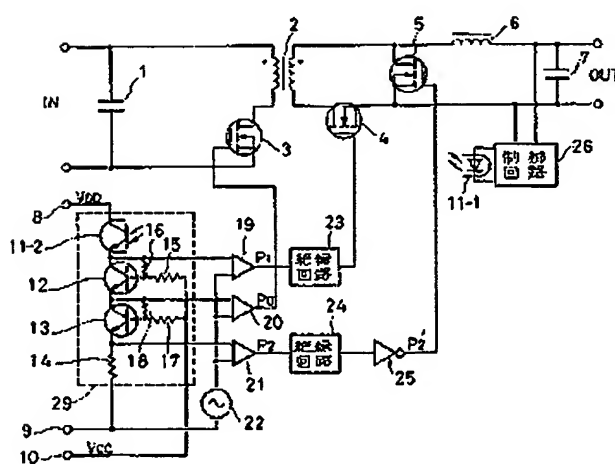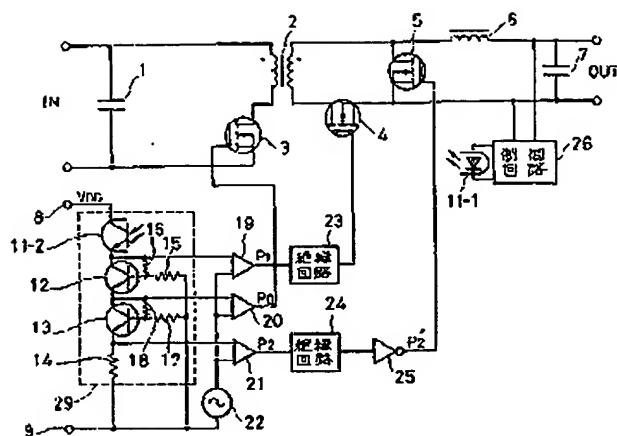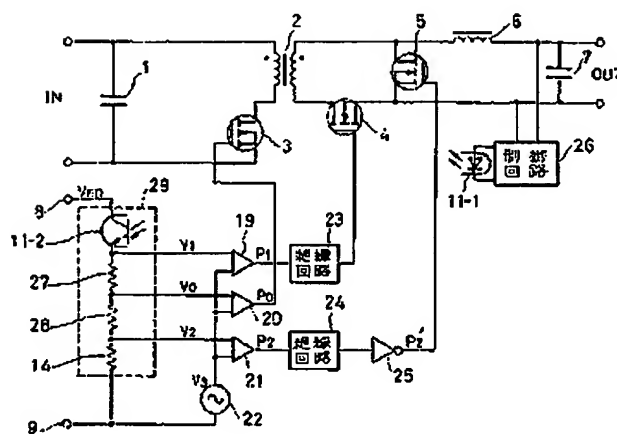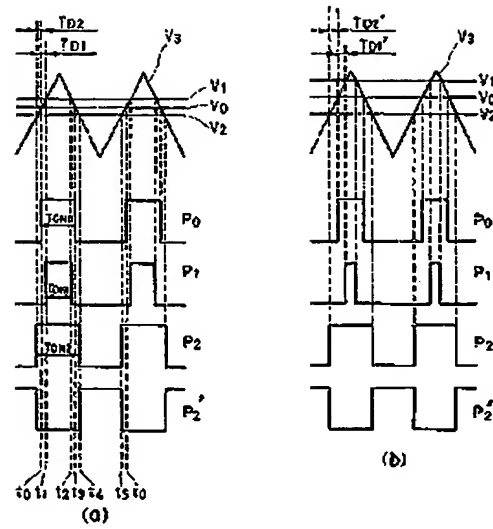
2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] A switching power supply circuit containing a transformer characterized by providing the following, a main-switch element which switches an upstream supply voltage of this transformer, a rectification smooth means which carries out rectification smoothness of the secondary output power of said transformer, and a switching device for synchronous detection by which on-off control is carried out by being prepared in this rectification smooth means and carrying out an abbreviation synchronization with on-off control action of said main-switch element A means to generate a from chopping sea A level shift means only for fixed level to carry out the level shift of the level of a direct-current control signal according to an output level of said rectification smooth means, and to generate level shift voltage A means which performs a level comparison with said direct-current control signal and said chopping sea, and makes this comparison pulse a switching pulse of said switching device for synchronous detection A means which performs a level comparison with said level shift voltage and said chopping sea, and makes this comparison pulse a switching pulse of said main-switch element

[Claim 2] A switching power supply circuit which contains in a secondary winding of said transformer the serial, 1st [by which on-off control is carried out by carrying out parallel connection and carrying out an abbreviation synchronization with on-off control action of said main-switch element], and 2nd switching devices for synchronous detection, respectively in a transformer characterized by providing the following, a main-switch element which switches an upstream supply voltage of this transformer, a rectification smooth means which carries out rectification smoothness of the secondary output power of said transformer, and this rectification smooth means A means to generate a from chopping sea A level shift means to carry out the sequential fixed level [every] level shift of the level of a direct-current control signal according to an output level of said rectification smooth means, and to generate the 1st and 2nd level shift voltage A means which performs a level comparison with said direct-current control signal and said chopping sea, and makes this comparison pulse a switching pulse of said 1st switching device for synchronous detection A means which performs a level comparison with said 1st level shift voltage and said chopping sea, and makes this comparison pulse a switching pulse of said

main-switch element, and a means which performs a level comparison with said 2nd level shift voltage and said chopping sea, and makes this comparison pulse a switching pulse of said 2nd switching device for synchronous detection

[Claim 3] Said level shift means is a switching power supply circuit according to claim 1 or 2 characterized by including a bias means which carries out bias of the 1st and 2nd transistors by which the series connection was carried out, and each transistors, such as this, to saturation operating state, respectively.

[Claim 4] Said level shift means is a switching power supply circuit according to claim 3 characterized by being the configuration that the series connection of a variable impedance element from which an impedance can change freely, and said 1st and 2nd transistors was carried out to this order between power supplies according to an output level of said rectification smooth means.

[Claim 5] a voltage level of a serial node of said variable impedance element and said 1st transistor -- said direct-current control signal level ****** -- a switching power supply circuit according to claim 4 characterized by things.

[Claim 6] A switching power supply circuit according to claim 4 or 5 characterized by this photo detector being said variable impedance element including a means to generate a lightwave signal according to an output level of said rectification smooth means, and a photo detector which receives this lightwave signal and presents an impedance according to this lightwave signal.

[Claim 7] A switching power supply circuit according to claim 6 characterized by including a photo coupler which supplies each of said switching pulse to the gate of a response switching device.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] Especially this invention relates to the switching power supply circuit which used the MOSFET synchronous detection circuit for the rectification section about a switching power supply circuit.

[0002]

[Description of the Prior Art] The synchronous detection method by MOSFET is adopted for the purpose of reducing the loss in the rectification section of a switching power supply circuit. Drawing 7 shows an example of a switching power supply circuit which used this synchronous detection method.

[0003] In drawing, it is impressed by the upstream of a transformer 2 by carrying out on-off control of the input power through MOSFET3 which is a main-switch element. It is rectified by MOSFETs 4 and 5 for rectification, and the alternating current power by which induction is carried out to secondary [of this transformer 2] is graduated by a choke coil 6 and the capacitor 7, and is changed into direct-current output voltage. In addition, 1 is an input capacitor.

[0004] Serial MOSFET4 for rectification and MOSFET5 for commutation of juxtaposition in a secondary winding (for flywheels) are formed in the secondary winding of a transformer 2, and MOSFETs 4 and 5, such as this, are controlled by the rectifier-circuit section to turn on and off fundamentally synchronizing with turning on and off of the main-switch element 3.

[0005] Furthermore, if it explains in full detail, when the main-switch element 3 is ON, MOSFET4 for rectification will serve as ON, and MOSFET5 for commutation will serve as OFF. Moreover, when the main-switch element 3 is OFF, MOSFET4 for rectification becomes off and MOSFET5 for commutation serves as ON.

[0006] That is, since MOSFET4 serves as ON and MOSFET5 becomes off when the main-switch element 3 is ON, supply of energy is performed from the input IN of a power supply to an output OUT. Moreover, when the main-switch element 3 is OFF, MOSFET4 becomes off, MOSFET5 serves as ON, and energy will be supplied to the output OUT of a power supply by the stored energy of a choke coil 6.

[0007] The actuation circuit which generates the on-off control pulse of the switching devices 3-5, such as this, is explained. Rectification smooth voltage is inputted into a control circuit 26, and the electrical signal according to this voltage level is changed into a lightwave signal by the light emitting device 11-1 of a photo coupler, and is impressed to a photo detector 11-2.

[0008] This photo detector 11-2 is a variable impedance element from which that impedance changes according to the strength of this light. It connects [this order] with power supplies 8 and 9 at a serial, and this variable impedance element 11-2 and resistance 27, 28, and 14 constitute the control signal output circuit 29.

[0009] output voltage V0 -V2 from each series-connection points, such as this, it becomes a control signal and draws -- having -- **** -- this etc. -- each -- control signal level V0 -V2 Chopping sea level V3 by the chopping sea generator 22 It is compared by the comparison machines 19-21, respectively.

[0010] Control signal level V1 of the serial node of a variable impedance element 11-2 and resistance 27 It is the chopping sea level V3 at a comparator 19. It is compared and is this comparison output PASURU P1. It is the gate control pulse of MOSFET4 through the insulating

circuit 23.

[0011] Control signal level V0 of a serial node with resistance 27 and 28 It is the chopping sea level V3 at a comparator 20. It is compared and is this comparison output PARUI P0. It is the gate control pulse of the main-switch element 3.

[0012] Moreover, control signal level V2 of a serial node with resistance 28 and 14 It is the chopping sea level V3 at a comparator 21. It is compared and is this comparison output pulse P2. It is control pulse P2 ' of MOSFET5 through the insulating circuit 24 and the inverter 25.

[0013] In addition, the photo coupler is used and the insulating circuits 23 and 24 are performing the insulation between secondary [of a transformer 2 / 1/secondary] with the photo coupler (11-1, 11-2) which transmits the output signal of a control circuit 26 to the control signal output circuit 29.

[0014] Next, actuation is explained. Drawing 8 is each part actuation wave form chart of the circuit of drawing 7 . The output signal of a control circuit 26 is transmitted to the photo-coupler light-receiving side 11-2 by the photo-coupler luminescence side 11-1. The impedance by the side of [11-2] photo-coupler light-receiving is changed. The voltage V1 of the node of the photo-coupler light-receiving side 11-2 and resistance 27, and the voltage V0 of the node of ** 27 and resistance 28, Voltage V2 of the node of resistance 28 and resistance 14 It is made to change and is the voltage V1, such as this, V0, and V2. Chopping sea V3 By comparing, it is the output pulse P1 of comparators 19, 20, and 21, P0, and P2. Pulse width is controlled.

[0015] At this time, it is V1 >V0 >V2. Since it is always maintained, relation is a pulse P1, P0, and P2. They are TON1, TON0, and TON2 about ON time amount. When it carries out, it is TON1 <TON0 <TON2. Relation is always maintained.

[0016] Pulse P1 The gate of FET4 is driven and it is a pulse P0. The gate of the main-switch element 3 is driven and it is a pulse P2. The gate of FET5 is driven by pulse P2 ' reversed with the inverter 25.

[0017] Here, it is a pulse P0. They are t0 and a pulse P1 about the time of day to turn on. They are t1 and a pulse P1 about the time of day to turn on. The time of day to turn off t2, Pulse P0 It is the time of day to turn off t3 The time of day which pulse P2 ' turns on t4, It is the time of day which pulse P2 ' turns off t5 It carries out and is referred to as t1-t0 =t3-t2 =TD1 (a pulse P0 and P1 between dead time) and t4-t3 =t0-t5 =TD2 (a pulse P0 and dead time between P2 ').

[0018] Time-of-day t0 -t1 Between and t2 -t3 In between, a main switch 3 has ON and off FET 4 and 5, and the load current flows by the root of the secondary winding of the internal diode -> transformer 2 of secondary-winding -> coil 6 -> load ->FET4 of a transformer 2.

[0019] Time-of-day t1 -t2 In between, ON and FET5 have a main switch 3 and off FET4, and the load current flows by the root of the secondary winding of the secondary-winding -> coil 6 -> load ->FET4 -> transformer 2 of a transformer 2.

[0020] Time-of-day t3 -t4 Between and t5 -t0 Main ISUTCHI 3 and FET 4 and 5 are off in between, and the load current flows by the root of the internal diode -> coil 6 of coil 6 -> load ->FET5. Time-of-day t4 -t5 In between, a main switch 3 and FET4 are [OFF and FET5] ON, and the load current flows by the root of coil 6 -> load ->FET5 -> coil ** 6.

[0021] FET4 to actuation of a main switch 3 and the delay of ON of five cause flow loss of FET 4 and 5, and loss by recovery current, when the load current flows to the internal diode of FET 4 and 5, and the off delay of FET 4 and 5 to actuation of a main switch 3 causes short circuit loss of a main switch 3 and FET 4 and 5 by the secondary-winding short circuit of a transformer 2.

[0022] So, at this example, it is a pulse P0. Just before turning off, it is a pulse P1. It turns off and is a pulse P0. It enables it to reduce loss resulting from the off delay of FET 4 and 5 to

actuation of a main switch 3 by turning off pulse P2 ', just before turning on. A pulse P0, P1, and P2 Effectiveness of a power supply will be made to max by forming the dead times TD1 and TD2 optimal in between.

[0023]

[Problem(s) to be Solved by the Invention] Although the optimal dead times TD1 and TD2 existed from MOSFET4 for synchronous detection to actuation of a main switch, and the time delay of actuation of five in the switching power supply circuit using this conventional actuation circuit for MOSFET synchronous detection, when the input condition of a power supply and load conditions changed, it becomes impossible to have maintained these optimal dead times TD1 and TD2, and there was a problem that the effectiveness of a power supply fell.

[0024] rated input voltage and the output current -- the effectiveness of a power supply -- ****** -- having -- as -- direct current voltage V0 which controls the pulse width of a main switch in order to extract the pulse width of a main switch when dead times TD1 and TD2 are set up (drawing 8 (a)), for example, the input voltage of a power supply rises (drawing 8 (b)) It goes up. Since the impedance by the side of [11-2] photo-coupler light-receiving becomes small at this time and the flowing current increases resistance 27 and 28, it is direct current voltage V0. The direct current voltage V1 which controls the pulse width of FET 4 and 5, and V2 A voltage difference increases, and dead times TD1 and TD2 increase to TD1' and TD2', and it becomes impossible to maintain the optimal dead time. Therefore, the flow time amount of the internal diode of FET 4 and 5 will increase, flow loss of FET 4 and 5 and loss by recovery current will increase, and the effectiveness of a power supply will fall.

[0025] The object of this invention is offering the switching power supply circuit which always enables maintenance of the optimal dead time, and can make power supply effectiveness good irrespective of change of I/O conditions.

[0026]

[Means for Solving the Problem] A main-switch element which switches an upstream supply voltage of a transformer and this transformer according to this invention, A means to be a switching power supply circuit containing a rectification smooth means which carries out rectification smoothness of the secondary output power of said transformer, and a switching device for synchronous detection by which on-off control is carried out by being prepared in this rectification smooth means and carrying out an abbreviation synchronization with on-off control action of said main-switch element, and to generate a from chopping sea, A level shift means only for fixed level to carry out the level shift of the level of a direct-current control signal according to an output level of said rectification smooth means, and to generate level shift voltage, A means which performs a level comparison with said direct-current control signal and said chopping sea, and makes this comparison pulse a switching pulse of said switching device for synchronous detection, A switching power supply circuit characterized by including a means which performs a level comparison with said level shift voltage and said chopping sea, and makes this comparison pulse a switching pulse of said main-switch element is obtained.

[0027] Furthermore, a main-switch element which switches an upstream supply voltage of a transformer and this transformer according to this invention, A rectification smooth means which carries out rectification smoothness of the secondary output power of said transformer, A means to be the switching power supply circuit which contains in a secondary winding of said transformer the serial, 1st [by which on-off control is carried out by carrying out parallel connection and carrying out an abbreviation synchronization with on-off control action of said main-switch element], and 2nd switching devices for synchronous detection in this rectification

smooth means, respectively, and to generate a from chopping sea, A level shift means to carry out the sequential fixed level [every] level shift of the level of a direct-current control signal according to an output level of said rectification smooth means, and to generate the 1st and 2nd level shift voltage, A means which performs a level comparison with said direct-current control signal and said chopping sea, and makes this comparison pulse a switching pulse of said 1st switching device for synchronous detection, A means which performs a level comparison with said 1st level shift voltage and said chopping sea, and makes this comparison pulse a switching pulse of said main-switch element, A switching power supply circuit characterized by including a means which performs a level comparison with said 2nd level shift voltage and said chopping sea, and makes this comparison pulse a switching pulse of said 2nd switching device for synchronous detection is obtained.

[0028]

[Function] Only fixed level carries out the level shift of the direct-current control signal level according to the rectification smooth voltage level which is a switching power supply output, level shift voltage is generated, and a comparison output pulse is obtained for each level of this level shift voltage and a direct-current control signal [chopping sea level / respectively]. Let comparison output pulses, such as this, be the on-off pulses of a main-switch element or the switching device for rectification.

[0029]

[Example] Hereafter, the example of this invention is explained using a drawing.

[0030] Drawing 1 is the circuit diagram of one example of this invention, and the same sign shows drawing 7 and an equivalent portion. Only a different portion from drawing 7 is explained and it omits about other configurations.

[0031] In the control signal output circuit 29, between power supplies 8-9, the photo detector 11-2 as a variable impedance element, NPN transistors 12 and 13, and resistance 14 carry out a series connection to this order, and are prepared in it. Between the base emitters of transistors 12 and 13, this etc. Bias is given by resistance 15 and 16, and 17 and 18 from the power supply VCC. By selection of the power supplies VCC and VDD (impression supply voltage to a power supply 8), such as this, and resistance 15-18 Each transistors 12 and 13 operate in a saturation region, and the voltage shift level which is therefore a voltage drop with transistors 12 and 13 serves as VCE1 and VCE2 (saturation voltage between collector emitters), and is maintained uniformly.

[0032] And voltage V1 of the serial point of a variable impedance element 11-2 and a transistor 12 Chopping sea V3 A level comparison is carried out by the comparator 19. moreover, transistor 12V1 VCE1 only -- voltage V0 which carried out the level shift Chopping sea V3 A level comparison is carried out by the comparator 20. furthermore, transistor 13V0 VCE2 only -- voltage V2 which carried out the level shift Chopping sea V3 A level comparison is carried out by the comparator 21.

[0033] Next, actuation is explained. Drawing 2 shows the wave of the circuit of drawing 1 of operation. Transistors 1 and 13 are VCE1 and VCE2 about the saturation voltage between collector emitters of transistors 12 and 13 here, respectively, although it drives according to the power supply 10 for transistor actuation and operates in a saturation state. It carries out.

[0034] The output signal of the output voltage control circuit 26 is transmitted to the photo-coupler light-receiving side 11-2 by the photo-coupler luminescence side 11-1. The impedance by the side of [11-2] photo-coupler light-receiving is changed. The voltage V2 of the emitter of the voltage V1 of the node of the collector of a transistor 12 and a transistor 12, the emitter of the

voltage V0 of the node of the collector of a transistor 13 and a transistor 13, and the node of resistance 14 is changed the photo-coupler light-receiving side 11-2, respectively. The voltage V1, V0, and V2, such as this, is compared with a chopping sea V3. Thereby, the pulse width of the output pulses P1, P0, and P2 of comparators 19, 20, and 21 is controlled.

[0035] Even if the impedance by the side of [11-2] photo-coupler light-receiving changes and the current which flows transistors 12 and 13 changes VCE1 and VCE2 It is fixed, the relation of V1=V0+VCE1 >V0>V2=V0-VCE2 is always maintained, and they are TON1, TON0, and TON2 about the ON time amount of pulses P1, P0, and P2. If it carries out The relation of TON1 =TON0-2TD1<TON0 <TON2 =TON0+2TD2 is always maintained (TD1; a pulse P0, the dead time between P1, the TD2; pulse P0, dead time between P2).

[0036] The gate of FET4 is driven by the pulse P1, the gate of a main switch 3 is driven by the pulse P0, and the gate of FET5 is driven by pulse P2' which reversed PASURU P2 with the inverter 25.

[0037] The rectification method of the load current in each time amount is the same as that of a circuit diagram 7 conventionally, and explanation is omitted.

[0038] Although only time amount TD 1 turns off a pulse P1 at the last time of day from the time of day which a pulse P0 turns off and pulse P2' is turned off at the time of day in front of ** by time amount TD 2 at this example from the time of day which a pulse P0 turns on It is TDLY about FET4 to actuation of a main switch 3, and the time delay of actuation of five. If it carries out TD1 and TD2 >=TDLY It is the voltage [VCE / VCE and / 2] 1 so that it may become. If it sets up, loss resulting from FET4 to actuation of a main switch 3 and the delay of OFF of five can be made into zero. Loss resulting from FET4 to actuation of a main switch 3 and the delay of ON of five can be made into min.

[0039] TD1 and TD2=TDLY It is the saturation voltage [VCE / VCE and / 2] 1 between collector emitters of transistors 12 and 13 so that it may become. It sets up by resistance 15 or 16 and resistance 17 or 18.

[0040] Dead times TD1 and TD2 are set up (drawing 2 (a)). here -- rated input voltage and the output current -- the effectiveness of a power supply -- ****** -- having -- as -- For example, although the direct current voltage V0 which controls the pulse width of a main switch 3 rises in order to extract the pulse width of a main switch 3 when the input voltage of a power supply rises (drawing 2 (b)) The difference with the direct current voltage V1 and V2 which controls the pulse width of direct current voltage 4 and FET [V0 and] 5 at this time is VCE1 and VCE2, respectively. Since it is fixed, dead times TD1 and TD2 are fixed, and can maintain the optimal dead time. Therefore, even if the input condition of a power supply and load conditions change, the always optimal dead time can be maintained and the effectiveness of a power supply can be maintained to max.

[0041] Drawing 3 shows the relation between the control signal level V1 and dead times TD1 and TD2 on the same conditions in each of the example of drawing 1 of this invention, and the example of conventional drawing 7 .

[0042] Input voltage 48V(IN) output voltage 3.3V (OUT) and output current 3.6A and switching frequency of 300kHz Although it considers as the Ford converter, the input capacitance of 1200pF and MOSFET of on resistance 45mohm are used for FET 4 and 5 and a dead time changes in proportion to the control signal level V1 like a property 31 in the conventional example, it turns out in this example that a fixed dead time is always obtained like a property 30.

[0043] In addition, although the saturation voltage of transistors 12 and 13 is used as an object for level shifts, it is clear that fixed level shift voltage may be obtained using zener diode.

[0044] <u>Drawing 4</u> is the circuit diagram of other examples of this invention, and is common-use-ized, using the power supply 8 (VDD) of the control signal output circuit 29 as bias power supply for actuation of transistors 12 and 13.

[0045] <u>Drawing 5</u> is the circuit diagram of the example of further others of this invention, it is a thing using PNP transistors 12 and 13, and <u>drawing 6</u> common-use-izes bias power supply for actuation of PNP transistors 12 and 13, such as this, with the power supply of the control signal output circuit 29.

[0046]

[Effect of the Invention] Since it has obtained with the voltage which carried out the fixed level shift of the control signal level for acquiring the on-off pulse of a switching device according to this invention as stated above The fixed dead time independent of the input condition and output condition of a power supply can be prepared in the on-off period of a main-switch element and the switching device for synchronous detection. Therefore, it is effective in becoming possible to always make into min loss which originates in the delay of MOSFET for synchronous detection of operation to actuation of a main-switch element, and power supply effectiveness becoming max.

TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the switching power supply circuit which used the MOSFET synchronous detection circuit for the rectification section about a switching power supply circuit.

[Description of the Prior Art] The synchronous detection method by MOSFET is adopted for the purpose of reducing the loss in the rectification section of a switching power supply circuit. Drawing 7 shows an example of a switching power supply circuit which used this synchronous detection method.

[0003] In drawing, it is impressed by the upstream of a transformer 2 by carrying out on-off control of the input power through MOSFET3 which is a main-switch element. It is rectified by MOSFETs 4 and 5 for rectification, and the alternating current power by which induction is carried out to secondary [of this transformer 2] is graduated by a choke coil 6 and the capacitor 7, and is changed into direct-current output voltage. In addition, 1 is an input capacitor.

[0004] Serial MOSFET4 for rectification and MOSFET5 for commutation of juxtaposition in a secondary winding (for flywheels) are formed in the secondary winding of a transformer 2, and MOSFETs 4 and 5, such as this, are controlled by the rectifier-circuit section to turn on and off fundamentally synchronizing with turning on and off of the main-switch element 3.

[0005] Furthermore, if it explains in full detail, when the main-switch element 3 is ON, MOSFET4 for rectification will serve as ON, and MOSFET5 for commutation will serve as OFF. Moreover, when the main-switch element 3 is OFF, MOSFET4 for rectification becomes off and MOSFET5 for commutation serves as ON.

[0006] That is, since MOSFET4 serves as ON and MOSFET5 becomes off when the main-switch element 3 is ON, supply of energy is performed from the input IN of a power supply to an output OUT. Moreover, when the main-switch element 3 is OFF, MOSFET4 becomes off, MOSFET5 serves as ON, and energy will be supplied to the output OUT of a power supply by the stored energy of a choke coil 6.

[0007] The actuation circuit which generates the on-off control pulse of the switching devices 3-5, such as this, is explained. Rectification smooth voltage is inputted into a control circuit 26, and the electrical signal according to this voltage level is changed into a lightwave signal by the light emitting device 11-1 of a photo coupler, and is impressed to a photo detector 11-2.

[0008] This photo detector 11-2 is a variable impedance element from which that impedance changes according to the strength of this light. It connects [this order] with power supplies 8 and 9 at a serial, and this variable impedance element 11-2 and resistance 27, 28, and 14 constitute the control signal output circuit 29.

[0009] output voltage V0 -V2 from each series-connection points, such as this, it becomes a control signal and draws -- having -- **** -- this etc. -- each -- control signal level V0 -V2 Chopping sea level V3 by the chopping sea generator 22 It is compared by the comparison machines 19-21, respectively.

[0010] Control signal level V1 of the serial node of a variable impedance element 11-2 and resistance 27 It is the chopping sea level V3 at a comparator 19. It is compared and is this comparison output PASURU P1. It is the gate control pulse of MOSFET4 through the insulating circuit 23.

[0011] Control signal level V0 of a serial node with resistance 27 and 28 It is the chopping sea level V3 at a comparator 20. It is compared and is this comparison output PARUI P0. It is the gate control pulse of the main-switch element 3.

[0012] Moreover, control signal level V2 of a serial node with resistance 28 and 14 It is the chopping sea level V3 at a comparator 21. It is compared and is this comparison output pulse P2.

It is control pulse P2' of MOSFET5 through the insulating circuit 24 and the inverter 25.

[0013] In addition, the photo coupler is used and the insulating circuits 23 and 24 are performing the insulation between secondary [of a transformer 2 / 1/secondary] with the photo coupler (11-1, 11-2) which transmits the output signal of a control circuit 26 to the control signal output circuit 29.

[0014] Next, actuation is explained. Drawing 8 is each part actuation wave form chart of the circuit of drawing 7 . The output signal of a control circuit 26 is transmitted to the photo-coupler light-receiving side 11-2 by the photo-coupler luminescence side 11-1. The impedance by the side of [11-2] photo-coupler light-receiving is changed. The voltage V1 of the node of the photo-coupler light-receiving side 11-2 and resistance 27, and the voltage V0 of the node of ** 27 and resistance 28, Voltage V2 of the node of resistance 28 and resistance 14 It is made to change and is the voltage V1, such as this, V0, and V2. Chopping sea V3 By comparing, it is the output pulse P1 of comparators 19, 20, and 21, P0, and P2. Pulse width is controlled.

[0015] At this time, it is V1 >V0 >V2. Since it is always maintained, relation is a pulse P1, P0, and P2. They are TON1, TON0, and TON2 about ON time amount. When it carries out, it is TON1 <TON0 <TON2. Relation is always maintained.

[0016] Pulse P1 The gate of FET4 is driven and it is a pulse P0. The gate of the main-switch element 3 is driven and it is a pulse P2. The gate of FET5 is driven by pulse P2 ' reversed with the inverter 25.

[0017] Here, it is a pulse P0. They are t0 and a pulse P1 about the time of day to turn on. They are t1 and a pulse P1 about the time of day to turn on. The time of day to turn off t2, Pulse P0 It is the time of day to turn off t3 The time of day which pulse P2 ' turns on t4, It is the time of day which pulse P2 ' turns off t5 It carries out and is referred to as t1-t0 =t3-t2 =TD1 (a pulse P0 and P1 between dead time) and t4-t3 =t0-t5 =TD2 (a pulse P0 and dead time between P2 ').

[0018] Time-of-day t0 -t1 Between and t2 -t3 In between, a main switch 3 has ON and off FET 4 and 5, and the load current flows by the root of the secondary winding of the internal diode -> transformer 2 of secondary-winding -> coil 6 -> load ->FET4 of a transformer 2.

[0019] Time-of-day t1 -t2 In between, ON and FET5 have a main switch 3 and off FET4, and the load current flows by the root of the secondary winding of the secondary-winding -> coil 6 -> load ->FET4 -> transformer 2 of a transformer 2.

[0020] Time-of-day t3 -t4 Between and t5 -t0 Main ISUTCHI 3 and FET 4 and 5 are off in between, and the load current flows by the root of the internal diode -> coil 6 of coil 6 -> load ->FET5. Time-of-day t4 -t5 In between, a main switch 3 and FET4 are [OFF and FET5] ON, and the load current flows by the root of coil 6 -> load ->FET5 -> coil ** 6.

[0021] FET4 to actuation of a main switch 3 and the delay of ON of five cause flow loss of FET 4 and 5, and loss by recovery current, when the load current flows to the internal diode of FET 4 and 5, and the off delay of FET 4 and 5 to actuation of a main switch 3 causes short circuit loss of a main switch 3 and FET 4 and 5 by the secondary-winding short circuit of a transformer 2.

[0022] So, at this example, it is a pulse P0. Just before turning off, it is a pulse P1. It turns off and is a pulse P0. It enables it to reduce loss resulting from the off delay of FET 4 and 5 to actuation of a main switch 3 by turning off pulse P2 ', just before turning on. A pulse P0, P1, and P2 Effectiveness of a power supply will be made to max by forming the dead times TD1 and TD2 optimal in between.

EFFECT OF THE INVENTION

[Effect of the Invention] As stated above, in this invention, it has obtained with the voltage which carried out the fixed level shift of the control signal level for acquiring the on-off pulse of a switching device. Therefore, the fixed dead time independent of the input condition and output condition of a power supply can be prepared in the on-off period of a main-switch element and the switching device for synchronous detection, and it is effective in becoming possible to always make into min loss which therefore originates in the delay of MOSFET for synchronous detection of operation to actuation of a main-switch element, and power supply effectiveness becoming max.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Although the optimal dead times TD1 and TD2 existed from MOSFET4 for synchronous detection to actuation of a main switch, and the time delay of actuation of five in the switching power supply circuit using this conventional actuation circuit for MOSFET synchronous detection, when the input condition of a power supply and load conditions changed, it becomes impossible to have maintained these optimal dead times TD1 and TD2, and there was a problem that the effectiveness of a power supply fell.

[0024] rated input voltage and the output current -- the effectiveness of a power supply -- ****** -- having -- as -- direct current voltage V0 which controls the pulse width of a main switch in order to extract the pulse width of a main switch when dead times TD1 and TD2 are set up (drawing 8 (a)), for example, the input voltage of a power supply rises (drawing 8 (b)) It goes up. Since the impedance by the side of [11-2] photo-coupler light-receiving becomes small at this time and the flowing current increases resistance 27 and 28, it is direct current voltage V0. The direct current voltage V1 which controls the pulse width of FET 4 and 5, and V2 A voltage difference increases, and dead times TD1 and TD2 increase to TD1' and TD2', and it becomes impossible to maintain the optimal dead time. Therefore, the flow time amount of the internal diode of FET 4 and 5 will increase, flow loss of FET 4 and 5 and loss by recovery current will increase, and the effectiveness of a power supply will fall.

[0025] The object of this invention is offering the switching power supply circuit which always enables maintenance of the optimal dead time, and can make power supply effectiveness good irrespective of change of I/O conditions.

[Means for Solving the Problem] A main-switch element which switches an upstream supply voltage of a transformer and this transformer according to this invention, A means to be a switching power supply circuit containing a rectification smooth means which carries out rectification smoothness of the secondary output power of said transformer, and a switching device for synchronous detection by which on-off control is carried out by being prepared in this rectification smooth means and carrying out an abbreviation synchronization with on-off control action of said main-switch element, and to generate a from chopping sea, A level shift means only for fixed level to carry out the level shift of the level of a direct-current control signal according to an output level of said rectification smooth means, and to generate level shift voltage, A means which performs a level comparison with said direct-current control signal and said chopping sea, and makes this comparison pulse a switching pulse of said switching device for synchronous detection, A switching power supply circuit characterized by including a means which performs a level comparison with said level shift voltage and said chopping sea, and makes this comparison pulse a switching pulse of said main-switch element is obtained.

[0027] Furthermore, a main-switch element which switches an upstream supply voltage of a transformer and this transformer according to this invention, A rectification smooth means which carries out rectification smoothness of the secondary output power of said transformer, A means to be the switching power supply circuit which contains in a secondary winding of said transformer the serial, 1st [by which on-off control is carried out by carrying out parallel connection and carrying out an abbreviation synchronization with on-off control action of said main-switch element], and 2nd switching devices for synchronous detection in this rectification smooth means, respectively, and to generate a from chopping sea, A level shift means to carry out the sequential fixed level [every] level shift of the level of a direct-current control signal according to an output level of said rectification smooth means, and to generate the 1st and 2nd level shift voltage, A means which performs a level comparison with said direct-current control signal and said chopping sea, and makes this comparison pulse a switching pulse of said 1st switching device for synchronous detection, A means which performs a level comparison with said 1st level shift voltage and said chopping sea, and makes this comparison pulse a switching pulse of said main-switch element, A switching power supply circuit characterized by including a means which performs a level comparison with said 2nd level shift voltage and said chopping sea, and makes this comparison pulse a switching pulse of said 2nd switching device for synchronous detection is obtained.

OPERATION

[Function] Only fixed level carries out the level shift of the direct-current control signal level according to the rectification smooth voltage level which is a switching power supply output, level shift voltage is generated, and a comparison output pulse is obtained for each level of this level shift voltage and a direct-current control signal [chopping sea level / respectively]. Let comparison output pulses, such as this, be the on-off pulses of a main-switch element or the switching device for rectification.

EXAMPLE

[Example] Hereafter, the example of this invention is explained using a drawing.

[0030] Drawing 1 is the circuit diagram of one example of this invention, and the same sign shows drawing 7 and an equivalent portion. Only a different portion from drawing 7 is explained and it omits about other configurations.

[0031] In the control signal output circuit 29, between power supplies 8-9, the photo detector 11-2 as a variable impedance element, NPN transistors 12 and 13, and resistance 14 carry out a series connection to this order, and are prepared in it. Between the base emitters of transistors 12 and 13, this etc. Bias is given by resistance 15 and 16, and 17 and 18 from the power supply VCC. By selection of the power supplies VCC and VDD (impression supply voltage to a power supply 8), such as this, and resistance 15-18 Each transistors 12 and 13 operate in a saturation region, and the voltage shift level which is therefore a voltage drop with transistors 12 and 13 serves as VCE1 and VCE2 (saturation voltage between collector emitters), and is maintained uniformly.

[0032] And voltage V1 of the serial point of a variable impedance element 11-2 and a transistor 12 Chopping sea V3 A level comparison is carried out by the comparator 19. moreover, transistor 12V1 VCE1 only -- voltage V0 which carried out the level shift Chopping sea V3 A level comparison is carried out by the comparator 20. furthermore, transistor 13V0 VCE2 only -- voltage V2 which carried out the level shift Chopping sea V3 A level comparison is carried out by the comparator 21.

[0033] Next, actuation is explained. Drawing 2 shows the wave of the circuit of drawing 1 of operation. Transistors 1 and 13 are VCE1 and VCE2 about the saturation voltage between collector emitters of transistors 12 and 13 here, respectively, although it drives according to the power supply 10 for transistor actuation and operates in a saturation state. It carries out.

[0034] The output signal of the output voltage control circuit 26 is transmitted to the photo-coupler light-receiving side 11-2 by the photo-coupler luminescence side 11-1. The impedance by the side of [11-2] photo-coupler light-receiving is changed. The voltage V2 of the emitter of the voltage V1 of the node of the collector of a transistor 12 and a transistor 12, the emitter of the voltage V0 of the node of the collector of a transistor 13 and a transistor 13, and the node of resistance 14 is changed the photo-coupler light-receiving side 11-2, respectively. The voltage V1, V0, and V2, such as this, is compared with a chopping sea V3. Thereby, the pulse width of the output pulses P1, P0, and P2 of comparators 19, 20, and 21 is controlled.

[0035] Even if the impedance by the side of [11-2] photo-coupler light-receiving changes and the current which flows transistors 12 and 13 changes VCE1 and VCE2 It is fixed, the relation of V1=V0+VCE1 >V0>V2=V0-VCE2 is always maintained, and they are TON1, TON0, and TON2 about the ON time amount of pulses P1, P0, and P2. If it carries out The relation of TON1 =TON0-2TD1<TON0 <TON2 =TON0+2TD2 is always maintained (TD1; a pulse P0, the dead time between P1, the TD2; pulse P0, dead time between P2).

[0036] The gate of FET4 is driven by the pulse P1, the gate of a main switch 3 is driven by the pulse P0, and the gate of FET5 is driven by pulse P2' which reversed PASURU P2 with the inverter 25.

[0037] The rectification method of the load current in each time amount is the same as that of a circuit diagram 7 conventionally, and explanation is omitted.

[0038] Although only time amount TD 1 turns off a pulse P1 at the last time of day from the time

of day which a pulse P0 turns off and pulse P2' is turned off at the time of day in front of ** by time amount TD 2 at this example from the time of day which a pulse P0 turns on It is TDLY about FET4 to actuation of a main switch 3, and the time delay of actuation of five. If it carries out TD1 and TD2 >=TDLY It is the voltage [VCE / VCE and / 2] 1 so that it may become. If it sets up, loss resulting from FET4 to actuation of a main switch 3 and the delay of OFF of five can be made into zero. Loss resulting from FET4 to actuation of a main switch 3 and the delay of ON of five can be made into min.

[0039] TD1 and TD2=TDLY It is the saturation voltage [VCE / VCE and / 2] 1 between collector emitters of transistors 12 and 13 so that it may become. It sets up by resistance 15 or 16 and resistance 17 or 18.

[0040] Dead times TD1 and TD2 are set up (drawing 2 (a)). here -- rated input voltage and the output current -- the effectiveness of a power supply -- ****** -- having -- as -- For example, although the direct current voltage V0 which controls the pulse width of a main switch 3 rises in order to extract the pulse width of a main switch 3 when the input voltage of a power supply rises (drawing 2 (b)) The difference with the direct current voltage V1 and V2 which controls the pulse width of direct current voltage 4 and FET [V0 and] 5 at this time is VCE1 and VCE2, respectively. Since it is fixed, dead times TD1 and TD2 are fixed, and can maintain the optimal dead time. Therefore, even if the input condition of a power supply and load conditions change, the always optimal dead time can be maintained and the effectiveness of a power supply can be maintained to max.

[0041] Drawing 3 shows the relation between the control signal level V1 and dead times TD1 and TD2 on the same conditions in each of the example of drawing 1 of this invention, and the example of conventional drawing 7 .

[0042] Input voltage 48V(IN) output voltage 3.3V (OUT) and output current 3.6A and switching frequency of 300kHz Although it considers as the Ford converter, the input capacitance of 1200pF and MOSFET of on resistance 45mohm are used for FET 4 and 5 and a dead time changes in proportion to the control signal level V1 like a property 31 in the conventional example, it turns out in this example that a fixed dead time is always obtained like a property 30.

[0043] In addition, although the saturation voltage of transistors 12 and 13 is used as an object for level shifts, it is clear that fixed level shift voltage may be obtained using zener diode.

[0044] Drawing 4 is the circuit diagram of other examples of this invention, and is common-use-ized, using the power supply 8 (VDD) of the control signal output circuit 29 as bias power supply for actuation of transistors 12 and 13.

[0045] Drawing 5 is the circuit diagram of the example of further others of this invention, it is a thing using PNP transistors 12 and 13, and drawing 6 common-use-izes bias power supply for actuation of PNP transistors 12 and 13, such as this, with the power supply of the control signal output circuit 29.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the circuit diagram of one example of this invention.
[Drawing 2] It is the wave form chart showing actuation of the circuit of drawing 1 , and (a) is each wave form chart when the input voltage of a power supply becomes high as for (b), when the I/O conditions of a power supply are rating.
[Drawing 3] It is drawing having compared and shown the relation between control signal level and a dead time in this invention and the conventional example.
[Drawing 4] It is the circuit diagram of other examples of this invention.
[Drawing 5] It is the circuit diagram of another example of this invention.
[Drawing 6] It is the circuit diagram of still more nearly another example of this invention.
[Drawing 7] It is drawing showing the conventional switching power supply circuit.
[Drawing 8] It is the wave form chart showing actuation of the circuit of drawing 7 , and (a) is each wave form chart when the input voltage of a power supply becomes high as for (b), when the I/O conditions of a power supply are rating.
[Description of Notations]
1 Input Capacitor
2 Transformer
3 Main-Switch Element
4 Five Switching device for synchronous detection
6 Choke Coil
7 Output Capacitor
11-1 Light Emitting Device
11-2 Photo Detector
12 13 Transistor
14 Resistance
15-18 Bias resistance
19-21 Comparator
22 Chopping Sea
23 24 Insulating circuit
25 Inverter